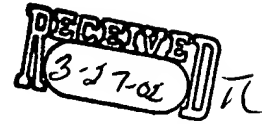


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generating coordinate data representing an initial rasterization starting point estimate when the region bits indicate that at least one of the sorted vertex data lies within the current tile being rendered and discarding the sorted vertex data of primitives that lie outside the boundary of the current tile being rendered; and

providing the initial rasterization starting point estimate to a rasterizer.

- B1
2. (Twice Amended) The method of Claim 1, further comprising:
generating an orientation bit representing an orientation of a line connecting the first and second vertices of the sorted primitive with respect to a line connecting the first and third vertices of the sorted primitive before generating the initial rasterization starting point coordinates.

3-13. Please CANCEL Claims 3-13 without prejudice or disclaimer of the subject matter contained therein.

- B2
14. (Amended) A circuit, comprising:
a sorting circuit operative to provide sorted vertex data in response to input data corresponding to vertices of a primitive, the vertex data being sorted in a coordinate-dependent fashion, the vertex data including x-coordinate and y-coordinate position information;
a region calculation circuit, coupled to the sorting circuit, operative to receive the sorted vertex data and to generate region bits representing the location of the sorted vertex data with respect to a current tile being rendered; and
an initial rasterization starting point circuit, coupled to the region calculation circuit, operative to generate an initial rasterization starting point coordinate in response to the region bits, the initial rasterization starting point circuit including a discard circuit operative to discard the vertex data of a primitive that lies outside the boundary defined by the current tile.
15. (Amended) The circuit of Claim 14, wherein the initial rasterization starting point circuit further includes a trivial accept circuit operative to provide the actual coordinates of the primitive as the initial rasterization starting point in response to the region bits.

18. (New) The circuit of Claim 17, wherein the boundary interception point generated by the intercept calculation circuit represents the initial rasterization point starting point coordinate.
19. (New) The circuit of Claim 14, further comprising an interception calculation circuit operative to provide a coordinate dependent initial rasterization starting point in response to the region bits and the sorted vertex data.
20. (New) The circuit of Claim 15, wherein the trivial accept circuit further comprises a logic gate coupled to a corresponding subset of the region bits.
21. (New) The circuit of Claim 20, wherein the logic gate is an AND gate.
22. (New) The circuit of Claim 14, wherein the region bits define the top edge, bottom edge, right edge and left edge of a current tile being rendered.
23. (New) The circuit of Claim 14, wherein the discard circuit further comprises a first AND gate having an output and inputs coupled to data representing the right most boundary of the current tile being rendered; a second AND gate having an output and inputs coupled to data representing the left most boundary of the current tile being rendered; and an OR gate having a first input coupled to the output of the first AND gate, a second input coupled to the output of the second AND gate, a third input coupled to data representing the top most boundary of the current tile and a fourth input coupled to data representing the bottom most boundary of the current tile, wherein the output of the OR gate provides a signal indicating whether the sorted vertex data lies within the current tile being rendered.
24. (New) The circuit of Claim 17, wherein the intercept calculation circuit clamps the x-coordinate and y-coordinate of the initial rasterization starting point to the boundary intercept points.
25. (New) The circuit of Claim 14, further including an orientation circuit, coupled to the region calculation circuit, operative to generate an orientation bit representing an orientation of a

line connecting the sorted first and second vertices with respect to a line connecting the sorted first and third vertices.

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C1 26. (New) The circuit of Claim 14, further including a comparator circuit operative to determine the relative positioning between the vertices of the primitive.

27. (New) A circuit for optimally determining an initial rasterization starting point, comprising:

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B a sorting circuit operative to provide sorted vertex data in response to input data corresponding to vertices of a primitive, the vertex data being sorted in a coordinate-dependent fashion, the vertex data including x-coordinate and y-coordinate position information;

a region calculation circuit, coupled to the sorting circuit, operative to receive the sorted vertex data and to generate region bits representing the location of the sorted vertex data with respect to a current tile being rendered; and

an initial rasterization starting point circuit, coupled to the region calculation circuit, operative to generate an initial rasterization starting point coordinate when the region bits indicate that at least one of the sorted vertex data lies within the current tile, the initial rasterization starting point circuit including a discard circuit operative to discard the vertex data of primitives whose vertices lie outside the boundary defined by the current tile.
